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JABIL

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Document Title Printed Circuit Board Fabrication Specifications

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FDC-RGRC-Document Approval

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	Printed Circuit Board Fabrication Specifications	

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Distribution List
Global Document Control Distribution

Rev	Author	Change Details
A to I	NA	*To see history of changes please click **HERE**.*
J	HS Tiu	Update 6.8.6.4 - to refer to IPC 4552 standard. Update 6.24.3.1 – to refer to IPC4553. Add 6.25 – Panel and Fab Drawing.

1. Purpose

1.1. This standard describes the detail requirements and specifications for the fabrication of rigid printed circuit boards (PCB) for all Jabil source suppliers of PCBs to Jabil.

2. Scope

2.1. This procedure pertains to all Jabil source suppliers and or PCB to Jabil worldwide plant who is with Surface Mount Technology & Through Hole process, with exception for customer supplied boards and customer's AVL parts.

2.2. The supplier is encouraged to perform a cost reduction, quality enhancement program along with their bids detailing all suggested improvements to enhance product first pass, first time yields. Cost savings after prove out will be shared as agreed upon between user and supplier.

2.3. The following controls are to be considered
- 2.3.1 Test and measurements on material/process requirements may be subcontracted to an outside laboratory.
- 2.3.2 Initial test measurements as may have previously occurred and certified on materials/processes replace the need of subsequent testing when applicable.

3. Definitions/ Terminology

3.1. SCM – Supply Chain Management
3.2. PCB – Printed Circuit Board
3.3. NPTH – Non-plated Through Hole
3.4. SMT – Surface Mount Technology
3.5. TH – Through Hole
3.6. CAD – Computer Aided Design

4. Responsibilities

Documentation Category	Selective

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4.1. It shall be the responsibility of the above listed managers to ensure that their divisions understand and adhere to this specification in carrying out their responsibilities.

4.2. It shall be the responsibility of the SCM PCB Commodity Team (Global Commodity Management & Global Supplier Development) personnel to ensure that all Jabil AVL and Jabil Strategy suppliers of Printed Circuit Boards to Jabil worldwide understand the contents of this document.

4.3. Is shall be the responsibility of the site Purchasing, Supplier Quality and Work-cell function to ensure that the site developed supplier and customer directed supplier who supplied PCB to Jabil understand the contents of this document.

5. Associated Documents

5.1. Reference Documents

5.1.1. Federal

QQ-N-290 Nickel Plating, Electrolytically Deposited
NSTA #3 Procedure for Pre-Shipment Testing Packaged Products
A-A-113 Tape, Pressure Sensitive

5.2. Supporting Documents

5.2.1. Industrial

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits
IPC 9191 General Requirements for implementation of Statistical Process Control
IPC-4103 Specifications for Base Material for High Speed/High Frequency Application
IPC-4562 Metal Foil for Printed Board Applications
IPC-4202 Flexible Bare Dielectrics for Use in Flexible Printed Circuitry
IPC-4203 Adhesive Coated Dielectric Films for Use as Cover Sheets for Flexible Printed Circuitry and Flexible Adhesive Bonding Films
IPC-4204 Flexible Metal-clad Dielectrics for Use in Fabrication of Flexible Printed Circuitry
IPC-6013 Qualification and Performance Specifications for Flexible Printed Boards
IPC-A-311 Process Controls for Photo-tool Generation and Use
IPC-D-325 Documentation Requirements for Printed Boards, Assemblies and Support Drawings
IPC-D-356 Bare Substrate Electrical Test Data Format
IPC-DR-572 Drilling Guidelines for Printed Boards
IPC-A-600 Acceptability of Printed Boards
IPC-OI-645 Standard for Visual Optical Inspection Aids
IPC-TM-650 Test methods Manual
IPC-9252 Requirements for Electrical Testing of Unpopulated Printed Boards
IPC-MI-660 Guidelines Incoming Inspection of Raw Materials Manual
IPC-7711/7721 Rework, Modification and Repair of Electronics Assemblies
IPC-MS-810 Guidelines for High Volume Micro-section
IPC-SM-840 Qualification and performance of Permanent Solder Mask
IPC-4101 Specification for Base Materials for Rigid and Multilayer Printed Boards
IPC-6011 Generic Performance Specifications for Printed Boards
IPC-6012 Qualification and Performance Specification for Rigid Printed Boards
IPC-6016 Qualification and Performance Specification for High Density Interconnect (HDI) Layers or Boards
IPC-4781 Qualification and Performance Specification of Permanent, Semi-Permanent Temporary Legend and/or Marking Inks

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IPC-9201 Surface Insulation Resistance Handbook
J-STD-003 Solderability Tests for Printed Boards
ASTM-B-488 Standard Specification for Electrodeposited Coatings of Gold for Engineering Uses
ASTM-E-345 Tension Test of Metallic Foil
ASTM-B-578 Gold Hardness Testing, Knoop Method
IPC1601 – Printed Board Handling and Storage Guidelines - (If request by Jabil end-customer or stated in PR/PO)
IPC-9151C - Process Capability, Quality and Reliability (PCQR2) Benchmark Test Standard and Database
IPC1710A – OEM Standard for Printed Board Manufacturers' Qualification Profile

5.3 Other Publications

UL 796 Standard for Safety, Printed Wiring Boards UL
94 Test for Flammability of Plastic Materials for Parts in Devices and Appliances
ISO-9002 Quality Systems-Model for Quality Assurance in Production, Installation and Servicing
NEMA L-11983 Industrial Laminated Thermosetting Products

6. Process

6.1. GENERAL REQUIREMENTS

6.1.1 For all criteria not specifically listed in this specifications or applicable drawings, all raw PCBs must conform to all of the listed specifications in 5.0 above using the latest revision available and follow the latest revision of IPC-6012 & IPC A- 600 specifications, Class II unless otherwise stated in the supplied data.

6.1.1.1.1 Printed Circuit Boards are classified by one of the three general Performance Classes as defined in IPC-6011.

6.1.1.1.2 Requirement Deviations, deviating from these heritage classifications shall be as agreed between user and supplier (AABUS).

6.1.1.1.3 Space and Military Avionics Deviations performance classifications are defined and listed in IPC-6012 (Appendix) standard. There are commonly referred to as Class 3/A.

6.1.2 All specifications outlined in this document are requirements unless otherwise stated in the individual PCB master (Fab) drawing or other supplied specification. Any other special requirements called out on the individual purchase order also take precedence over this specification and individual PCB drawing documentation.

6.1.2 Manufacturability study – It is the responsibility of the supplier to conduct a thorough review of the customer's Gerber files, artwork, and media for manufacturability in the supplier's process and conformance to the applicable specifications. Jabil must be advised in writing *(Engineering Queries, EQ and Product/Process Change Notice - PCN)* (in advance of manufacturing) of any changes, corrections, or recommendations to ensure conformance to the applicable specifications as herein outlined. For clarity, all written communications should be forwarded to the buyer who is authorized to issue the purchase order with appropriate copies to work-cell support staff. Supplier must receive written approval from Jabil before changes are made.

6.1.4 The order of precedence for the manufacture of PCBs supplied to Jabil shall be as follows:

6.1.4.1 The Purchase Order

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6.1.4.2 Printed Circuit Board Drawing (master, Fab), including Gerber data and artwork film
6.1.4.3 Any supplied Jabil or Jabil customer specifications
6.1.4.4 This Specification, 4-MT60-1000-001 latest revision
6.1.4.5 Documents referred to in this specification above

6.1.5 All notes are "unless otherwise specified".

6.1.6 This standard includes test means for measuring and assuring product quality. These test means may be substituted with equivalencies as agreed upon between supplier and user.

6.2. MATERIAL SPECIFICATIONS

6.2.1 Single-Sided Boards – The base material for single sided printed circuit with UL- 94V-0 flame rating per IPC-4101.

6.2.2 Double-Sided Boards – The base material shall be glass-fiber base, epoxy resin with UL-94V-0 flame rating per IPC-4101. Thickness shall be as specified on the printed circuit board master (Fab) drawing.

6.2.3 Multilayer Boards

6.2.3.1 The base material for internal (core) layers & external layer shall be glass-fiber base, epoxy resin with UL-94V-0 flame rating per IPC-4101.
6.2.3.1.1 When "foil lamination" is used for external layers, copper foil shall be designated per IPC 4562. **NOTE: Exceptions to material type above, so as to accommodate quality, value and cost interests for a specific application, may be as agreed upon in writing between user (Jabil) and supplier. Further exception can occur as indicated on the master drawing for the fabrication of the printed circuit board.**

6.2.4 The B-stage material for dielectric layers shall be pre-impregnated glass-fiber, epoxy resin with UL-94V-0 flame rating; type GF per IPC 4101. Color shall be natural. Thickness of the dielectric layers must be such that overall composite thickness, as specified on the master (Fab) drawing or other supplied specifications shall be maintained. 6.2.4.1 The B-stage material shall be tested per IPC 4101 unless specified with other supplied specifications.

6.2.5 Bonding of the multilayer boards shall be such that separation shall not occur and the copper plated-through holes (PTH) do not crack (at 100 to 200, magnification examination) when tested according to IPC-TM650, 2.1.1 unless specified with other supplied requirement.

6.2.6 Thermal Resistance & Stress - The Thermal Resistance shall be conducted accordance with IPC-TM650 method 2.6.27 and Thermal Stress shall be conducted accordance with IPC-TM650 method 2.6.28.

6.2.7 The base material referred to in Paragraphs 6.2.1 and 6.2.2 of this specification shall be C stage material in the fully cured condition. As a minimum, the cure must be stated in terms of the Tg (Glass Transition Point). The supplier may use certificates as obtained from their laminate supplier with copies of the certification supplied to Jabil Circuits Inc. by attaching copies of the Certificate of Conformance to the final inspection document with each shipment. Additional test demonstrating laminate cure may be used such as: IPC-TM650 2.4.24,

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6.2.7.1 Thermal Mechanical Analyzers (TMA) to verify CTE in X, Y, and Z directions. Values must agree with the initial material supplier's technical specification sheets.

6.2.7.2 Differential Scanning Calorimetry (DSC) 6.2.7.3 Thermal Gravitation Analysis (TGA)

6.2.8 A coupling agent (adhesion promoter) such as silane shall be bonded onto the glass fabric strands so as to enhance the glass-to-epoxy bond. This coupling agent thickness shall not exceed 5 microns.

6.2.9 Glass fabric weaves tension and other textile pattern configurations and parameters once selected shall be consistently used and compliance controlled. Any changes of stack-up shall obtain customer written approval through ECN process.

6.3. DRILLING PROCESS

6.3.1 All hole diameter specified on the master (Fab) drawing are finished sizes or as specified in the data pack.

6.3.2 All tooling holes shall be non-plated through holes (NPTH) unless otherwise specified on the master drawing.

6.3.3 The data in the NC drill file is sorted by holes' size. The data is not optimized. It is the supplier's responsibility to optimize the NC data.

6.3.4 The minimum annular ring for external layers shall follow the master (Fab) drawing and other supplied specifications followed by IPC standard. The supplier shall be responsible for providing substantiating data for compliance of internal interconnects.

6.3.5 All holes are to be drilled in accordance with the supplier's knowledge of capability studies to maintain all NPTH's. As it is encouraged to drill all holes at primary drill, the option is left to the supplier to optimize the process for greatest manufacturability. If a second drill operation is elected; the supplier is to maintain the specifications for geometric dimension & tolerancing (GDT) found in this specification, Paragraph 6.3.2.

6.3.6 HDI design, via holes annular ring must comply with IPC-6016 and all other requirements of IPC-6012 & IPC A600. No breakout is allowed for via annular ring for internal and external layers.

6.3.7 Drilling halo, fracturing, lifting of the copper cladding or drilling burrs acceptance/rejection shall according to IPC-A-600 unless specified in master (Fab) drawing and other supplied specifications.

6.3.8 An accumulation of resin tear-out and the holes' wall roughness shall meet the customer supplied specification when supplied or IPC standard from the edge plane of the nominal drilled hole, when measured in micro-section at 200X.

6.3.9 For back drill process, stub length (this should be minimized without impact to the effective length), burrs (should be no obvious metal burr under 10 X visual inspection.), hole shift (1st vs back drill, should be within 0.127 mm round), and no exposed copper for other inner layers, no glass fiber pull out or separation in laminate due to improper drilling parameter and etc.

6.4. PLATING SPECIFICATIONS

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6.4.1 Copper Plating – All electrolytically deposited copper plating shall meet the requirements of specifications provided, or minimum thickness shall in accordance with IPC 6012, (class 1 – 20 um, class 2 – 20um & class 3 – 25um). Purity shall not be less than 99.5%

6.4.1.1 Elongation – An elongation test for ductility of copper plating shall be run per IPC-TM650 (2.4.18.1) and Mil specification. The customer drawing requirement will take precedence. An outside laboratory may perform the test; the plating shall be performed by the supplier's production process used to make the production boards. These records should be available for review by any Jabil personnel when requesting the data.

6.4.2 Tin-Lead Plating – All electrolytically deposited tin-lead plating shall contain a minimum of 60% and a maximum of 70% tin. Tin-Lead coatings shall meet IPC/EIA J-STD-003 and or other supplied requirement.
6.4.2.1 Solder Float Test – Shall be conducted in accordance with MIL-PRF- 55110 or IPCTM-650.
6.4.2.2 Solderability of the finished circuit board shall be performed per J-STD- 003.

6.4.3 Gold Plating – If not specified on the customer master (Fab) drawing or other supplied specifications, contact fingers and immersion gold plating shall be gold plated per IPC-6012.

6.5. PLATED-THROUGH HOLES

6.5.1 Copper plating in the plated through holes shall be electrolytically produced in accordance with Paragraph 6.4.1 of this specification.

6.5.2 The minimum plated copper thickness in the plated-through holes shall meet IPC-A-600 or other specified supplied requirement.

6.5.3 The plating thickness measurements shall be taken per IPC-TM-650.

6.5.4 Bonding of multilayer boards shall be such that separation shall not occur and plated through holes do not crack when tested to IPC-TM-650. Testing shall occur once per production run. Evidence of completion of this testing shall be documented.

6.5.5 After preconditioning in a circular air oven at 110 degrees C for 3 hours, copper plating shall meet the thermal requirements of MIL-PRF-55110. 6.5.6 Nail-heading shall follow IPC-A600 if not specified by the master (Fab) drawing and/or supplied requirement documents.

6.6. ETCHING

6.6.1 **"Tear Dropping" for increased manufacturability is permissible providing the finished etched product does not violate spacing requirements of the master drawing, supplier shall obtain Jabil and Jabil customer approvals for any add or change.**

6.6.3 The acceptance of (scratches, dents, etc) shall meets the master (Fab) drawing and/or other supplied specification. If not stated, shall accordance with IPC-A- 600.

6.6.4 Peel strength of external conductors after solder float shall meet the IPC-TM-650.

6.6.5 Minimum annular ring on any external layer shall meet IPC-6012 or the master (Fab) drawing and or supplied specification.

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6.7. SOLDER MASKING

6.7.1 Solder mask shall be applied over bare copper to the component and solder sides of the printed circuit boards unless stated on the master (Fab) drawing or other supplied specifications by using mechanical screen printing techniques utilizing thermal type inks or photo process utilizing photoimageable type inks applied by flood screening, curtain coating, or electrostatic spray techniques. The supplier is allowed ink selection providing the supplier shall use UL recognition ink for the selection made and unless otherwise stated on the master (Fab) drawing, the color shall be green unless specified on the master (Fab) drawing or other supplied specifications.

6.7.2 Solder mask shall meet the physical requirements of IPC-SM-840 (abrasion resistance, solvent resistance, etc.).

6.7.3 Thickness of the solder mask shall meet IPC-SM-840 & IPC-A-600. Unless otherwise stated on the master drawing, the color shall be green.

6.7.4 Upon the selection of the solder mask material for a given part number, the manufacturer shall Not change the type without prior written approval from Jabil Circuit. Consecutive lots shall have the same material selection as that which the manufacturer used for the first lot manufactured.

6.7.5 Solder mask registration shall allow IPC-SM-840 & IPC-A-600 and no masking material allowed on the pad solder area.

6.7.6 The manufacturer is allowed to expand or decrease the Gerber data solder mask artwork to satisfy the requirements of this specification.

6.7.7 The solder mask shall be capable of withstanding the thermal test as per IPC-TM- 650 #2.6.7.3.

6.7.8 The solder mask shall withstand the tape test which uses one-inch cellophane tape conforming to Type I, Class A; of IPC-A-600 Standard, with no removal or lifting of mask and mask edge from conductor surface or base laminate.

6.7.9 There shall be no haze (discoloration), blistering, cracking, peeling or flaking of the solder mask and the mask shall be free of internal voids and other inclusions or discoloration spots must meet IPC-A-600.

6.7.10 Touch-up of the solder mask is acceptable, unless otherwise stated in supplied specifications not excessive (as agreed upon), and if the application is uniform and neat in appearance.

6.7.11 Solder mask "tenting" filled via the filled via solder mask thickness shall less than 50 micro measured above copper land and minimum filled 50%. (Unless otherwise stated in supplied specifications)

6.8. FINAL METAL FINISHES

6.8.1 Plating materials shall be in accordance with the specification herein. Selection and location of plating materials used on the conductive pattern shall be in accordance with the master (Fab) drawing or other supplied specifications herein. Prior to plating any finish, the copper surface shall pass the water break test.

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6.8.2 Hot Air Solder Level (HASL)

6.8.2.1 Thickness shall be in accordance with IPC-6012 unless specified in the master (Fab) drawing or other supplied specifications.

6.8.2.2 Solder coatings shall be a minimum of 60% and a maximum of 70% tin, with the remainder lead.

6.8.2.3 De-wetting of solder coatings shall not exceed 5% of the total conductor surface area. Non-wetting of solder coatings shall not be acceptable.

6.8.2.4 Lead free HASL shall meet the requirements RoHS if specified.

6.8.3 Fused Tin-Lead

6.8.3.1 Fused Tin-Lead shall cover all exposed copper on the traces and pads.

6.8.3.2 Fusing shall be ductile, smooth, continuous, and free of defects determined to the wetting action of solder.

6.8.3.3 The minimum thickness after reflow shall be average of 0.0003 inch, with no single measurement less than 0.0001 inch.

6.8.4 Electrodeposited Tin-Lead

6.8.4.1 All Electrodeposited Tin-Lead shall meet the composition (50% to 70% tin) requirement of ASTMB-579, accordance to IPC-6012 3.2.7.2.

6.8.4.1 Lead shall be fused unless otherwise noted in the master (Fab) drawing or other supplier specifications.

6.8.5 Organic Solderability Preservative (OSP)

6.8.5.1 The OSP to be used on Jabil product shall meet the RoHS and lead free requirements. Unless specified by supplied specifications.

6.8.5.2 OSP-coated PCBs with gold finger connectors shall have all OSP residues removed from the gold fingers.

6.8.5.3 Operators who come into direct contact with OSP-coated PCBs shall wear non-permeable gloves.

6.8.5.4 Gold finger PCBs shall be recoated with OSP no more than one complete cycle through the OSP process line.

6.8.5.5 Any other OSP-coated PCB shall be recoated with maximum of two complete cycles through the OSP process line.

6.8.5.6 Test per the OSP chemistry manufacture's recommended test procedure and frequency.

6.8.6 Electroless Nickel Immersion Gold

6.8.6.1 All copper features as designated, shall be finished with electroless nickel/immersion gold suitable of soldering as specified in the IPC-4552.

6.8.6.2 The nickel/gold plating is to be applied after solder mask.

6.8.6.3 The nickel plating thickness shall be a minimum of 118 micro inches and maximum of 236 micro inches [3 to 6 µm].

6.8.6.4 Unless specified the master (Fab) drawing and other supplied specifications, the gold plating thickness shall follow the IPC-4552.

6.8.6.5 The manufacturer shall use adequate visual inspection to ensure that the product is free of discoloration, streaks, and non-uniformity of color.

6.8.6.6 The manufacturer shall implement adequate inspection steps and control plans to ensure the solderability of the product. All solderability is to meet or exceed the requirements of IPC-6012, Class 2, section 3.3.6 and IPC-TM-650.

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6.8.7 Electrolytic Nickel/Gold Plating (Gold Edge Connectors)

6.8.7.1 When specified by the master (Fab) drawing or other supplied specifications, PCB edge contacts shall be fabricated in accordance with IPC-A-600, Class 2, Section 2.7.1.

6.8.7.2 Board edge contacts shall be manufactured with electrolytic gold plating over nickel plating over copper unless otherwise stated by the supplied specifications.

6.8.7.3 Adhesion of gold plating shall be determined by IPC-TM-650, Method 2.4.10.

6.8.7.4 Gold plating hardness testing shall comply with the requirements of ASTM-B-578.

6.8.7.5 There shall be no peeling or flaking of golf plating when tape tested in accordance with IPC-A-600.

6.8.7.6 Board Edge Critical Contact Area

6.8.7.6.1 All PCB edge contacts by definition have what is considered a critical contact area. If the critical contact area is not detailed in the master (Fab) drawing or other supplied specification, the critical contact area shall be as defined within this section.

6.8.7.6.2 The plating in the critical contact area shall not contain any exposed base metal pinholes, tape residue, or solder mask. **Tape residues or flux is not allowed on any area on or around the gold fingers.**

6.8.7.6.3 The plating in the critical contact area shall not contain any scratch whose greatest dimension in width exceeds 0.003 inch.

6.8.7.6.4 Pits, dents, and depressions are acceptable if they do not exceed 0.006 inch in their longest dimension and there are not more than 3 per land area and do not appear on more than 30% of the lands.

6.8.7.6.5 The plating in the critical contact area shall be smooth (not contain any solder splash or silver) and uniform in appearance. No presence of staining, organic or non-organic contamination is permitted.

6.8.7.6.6 There shall be no burred edges allowed at the edge contact area as a result of robber bars or plating bars.

6.8.7.6.7 Gold Porosity Testing shall be performed regularly as a process control and a suitable process norm shall be established. IPC-TM-650 Test Methods Manual has listed 3 methods for gold porosity test:

(1) Test method 2.3.24 Porosity of Gold plating (chemical method). This method provides procedures to determine the porosity of gold plating both copper and nickel surface by chemical means.

(2) Test method 2.3.24.1 Porosity Testing of Gold Electrodeposited on a Nickel Plated Copper Substrate Electrographic Method. This method provides a procedure for testing the porosity of gold electroplated from an alkaline (cyanide), acid, or neutral gold plating solution on a nickel substrate in contact with golf deposit.

(3) Test method 2.3.24.2 Porosity of Metallic Coatings on Copper Base Alloys and Nickel (Nitric acid vapor test). This method is the preferred procedure for the testing of porosity of gold plating. The manufacture may choose any one of the three methods. Once a method has been selected, the supplier is required to maintain this method on all Jabil Product without exception. Any change of procedure must have prior written approval.

6.8.7.7 Board Edge Chamfer and Bevel Requirements – The manufacture must refer to the master fabrication drawing for required chamfer angle and other dimensions. The bevel and flat edges of the chamfer shall be smooth and free of burrs.

6.9. SILK SCREEN REQUIREMENTS

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6.9.1 Silk screen shall be in accordance with the Jabil supplied Gerber data or other supplied specifications.

6.9.2 The ink used by the manufacturer shall be high temperature, permanent, and nonconductive ink. Unless otherwise stated on the master (Fab) drawing or other supplied specification, the color is to be white. It shall be accordance with IPC- 4781 specification.

6.9.3 Silk screen ink must not be present on pads, annular rings, or any other surface feature intended for soldering. In the event the artwork furnished violates these criteria, the manufacturer must notify the appropriate Jabil buyer prior to production.

6.10. ELECTRICAL TEST REQUIREMENTS

6.10.1 All PCBs shall be 100 percent electrically tested for short circuits and opens by the PCB manufacturer before shipment to the Jabil facilities. Electrical testing shall include all plated-through component holes and any SMT surface connections required and all PCB edge connector contacts per the supplier net list file. A PCB must pass the electrical test according to the data-derived test program in a single test cycle, unless for quick turn order that can be tested with flying probe tester.

6.10.2 Electrical test for PCBs consist of the following:

6.10.2.1 The continuity ("opens") test that verifies that each circuit trace network is intact. Connections that exhibit a higher resistance than the Pass/Fail threshold as found in IPC-9252 fail the test (and must be reported as "open").

6.10.2.2 An isolation ("shorts") test that verifies each circuit trace network is sufficiently isolated from the rest of the trace networks on the PCB. The test system grounds all networks, except the one to be tested, then measures the resistance between the tested network and ground. If the measured resistance is lower than the Pass/Fail threshold as found in IPC-9252, the network fails the test and must be reported as a "short".

6.10.3 Fault coverage for PCB electrical test must be 100 percent. All networks on the PCB must be tested for continuity and isolation.

6.10.4 Insulation and isolation resistance shall be tested on a sample lot of each manufacturing lot. IPC 6012 & IPC 9252 standard shall apply. Unless otherwise specified in supplied specifications.

6.10.5 All boards, which have passed testing, shall be marked with "ET" in permanent, nonconductive ink. The stamp shall be placed in a location free of surface mount pads, test points, fiducials, or other markings. For manufactured product in array form, all PCBs are to be stamped which have passed, unless specified and or obtain approved from appropriate Jabil buyer placing the purchase order.

6.10.6 Multilayer boards with internal VCC and GND must pass a high potential (Hi-Pot) test as per the master (Fab) drawing or other supplied specifications. And or follow by IPC-6012 & IPC-TM650 2.5.71.

6.10.7 All PCBs shall be tested according to the requirements of IPC-9252, except as noted below.

6.10.7.1 No defective parts are acceptable on multiple PCB arrays **(No X-out)**, unless otherwise stated by the master fabrication drawing (or a written deviation from the Jabil buyer).

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6.10.7.2 Open and short circuit resistance threshold shall follow the master (Fab) drawing and other supplied specifications follow by the IPC standard.

6.10.7.3 Unless otherwise stated by the master (Fab) drawing and or other supplied specification, the isolation test shall be accordance with IPC- 9252 & IPC-6012 specifications

6.10.7.4 The test system shall incorporate a means of limiting the energy delivered to failing (shorted) networks; so that tested products are not damaged.

6.10.7.5 The electrical test program and test fixture shall be generated from either the supplied Gerber or CAD database files. **The "golden PCB/self-learn/reference test" method of test program generation is NOT acceptable.**

6.10.7.6 Any PCB reworked or repaired in any way after an electrical test shall be subjected to an entirely new electrical test.

6.11. MARKINGS

6.11.1 Markings shall be placed on the solder side of the PCB in locations indicated on the master fabrication drawing. Markings shall be legible and include, but not limited to the following:

6.11.1.1 Manufacturer's logo, Date Code (WWYY), and lot or job number that is traceable to the manufacturer's process and material records.

6.11.1.2 Manufacturer's UL registered marking, as specified in the UL Recognized Component Index (UL 796).

6.11.1.3 The appropriate part number as indicated on the master (Fab) drawing or other supplied specification.

6.11.2 The ink utilized in stamping must be non-conductive, permanent (must withstand all Jabil processes without degradation), and in a contrasting color for high visibility. In the event the stamping ink is conductive, it must not be applied across circuit traces (even though solder mask is present) or any other area that could result in immediate or latent electrical failures.

6.12. DE-PANELIZATION – FINAL PROFILING

6.12.1 NC Route

6.12.1.1 PCBs shall be NC routed out of the panels unless otherwise stated by the master (Fab) drawing or other supplied specification. Routed PCBs shall meet the following requirements.

6.12.1.1.1 No chipping of solder mask is permissible after the routing process.

6.12.1.1.2 No exposed copper shall be permissible along PCB outside routing edge.

6.12.1.2 The outside routing dimension of the finished PCB shall be per master (Fab) drawing or other supplied specifications.

6.12.2 PUNCHING

6.12.2.1 All punching shall meet IPC or other supplied specifications.

6.12.3 SCORING

6.12.3.1 Unless otherwise stated on the master (Fab) drawing or other supplied specifications, the scoring must meet the following criteria (based upon 0.062 inch PCB overall thickness only). Web thickness shall be 0.020 +/- 0.005 or in accordance with the master (Fab) drawing. Misalignment from top to bottom score lines to be +/- 0.005 inch.

6.12.3.2 For boards, which are not 0.062-inch nominal, the manufacturer shall manufacturer in accordance with the master (Fab) drawing or other supplied specifications.

6.12.3.3 Unless specified in fabrication drawing, the V-scoring angle and tolerance shall be 30 +/- 5 degree.

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6.13. BOARD DIMENSIONS AND TOLERANCES

6.13.1 Unless otherwise specified, PCB dimensions and tolerances must adhere to the master (Fab) drawing or other supplied specifications.

6.13.2 Hole's Size and Hole Pattern Accuracy – Hole sizes and tolerances shall be in accordance with the master (Fab) drawing or other supplied specifications. Burrs or rough plating in the PTH holes shall not reduce the holes' diameter below the minimum defined in the master fabrication drawing.

6.13.3 Registration (Internal & External) – The registration shall meet the IPC-6012 specification or other supplied specifications.

6.14. WARP AND TWIST

6.14.1 PCBs shall have a maximum bow warp and twist (over their entire surface) of 0.007 inch per inch measured on the diagonal with a **maximum of 0.090 inch**, unless otherwise specified on the master (Fab) drawing or other supplied specifications. Warp and twist shall be measured in accordance with IPC-TM-650, Method 2.4.2.2.

6.14.2 When the finished PCB is passed over the wave solder machine per IPC-J-STD- 003, warpage shall be maintained within the limits the value shown in 6.14.1 of this specification.

6.15. VISUAL EXAMINATION AND INSPECTION

6.15.1 Unless otherwise stated, PCBs used by Jabil shall meet or exceed the requirements of the latest revisions of IPC-6012 and IPC-A-600, Class 2 criteria. PCBs should be visually examined for anomalies at a magnification of 1.75X. Magnification of minimum 7X shall be used for micro-BGA areas. If the conditions are abnormal, they should be verified at progressively higher magnification (up to 40X) to confirm whether or not it is an actual nonconformance.

6.15.1.1 **PCB Markings** shall be made by the same process used to produce trace patterns where at all possible pending acceptable area and is the preferred Jabil method. Markings must be made only in certain designated areas provided on the master (Fab) drawing or other supplied specifications and must include (at least) the following information:

a. Part Number and revision level
b. Date of manufacture (4 digit date code) WW-YY.
c. Supplier's UL logo and symbol for direct support of live current carrying parts
d. Flame retardant rating-PCB manufacturer shall certify that the substrate conforms to 94V-0, Flammability rating and mark the PWB accordingly with the UP listed Traceability Emblems, per UL 796 Standard for Safety
e. Country of origin shall be indicated by filling in the blank after the text "MADE IN_____" on the artwork information provided by Jabil
f. Visual acceptance criteria for marking shall be in accordance with IPC-A-600, Class 2, Section 2.8.

6.15.1.2 Solderability – Solderability testing shall be in accordance with IPC- 6012, Class 2, and section 3.3.6 or Category 2 of J-STD-003.

6.15.1.3 Plating adhesion shall meet the requirements of IPC-6012, Class 2, Section 3.3.7. The adhesion of the plating shall be tested in accordance with IPC-TM-650, method 2.4.1.

6.16. AUTOMATED OPTICAL INSPECTION (AOI)

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6.16.1 Automated optical inspection (AOI) using CAD referenced files are required on all inner-layer and outer-layer photo tools prior to release to production.

6.16.2 AOI using CAD reference files is required on all Jabil inner signal layers and preferred on inner layer plane and outer layers. Any deviation to the AOI requirement must be obtained from the appropriate Jabil Work-cell prior to quoting or manufacturing Jabil boards.

6.17. SURFACE INSULATION RESISTANCE (S.I.R.) TESTING

6.17.1 When required as stated in master (Fab) drawing/document or other supplied specifications, the S.I.R test must be conducted per IPC-TM-650 #2.6.3.7.

6.17.1.1 In the event that the panel utilization does not allow for sufficient area for coupon implementation, the supplier must utilize suitable and approved means (test coupon meeting IPC standards) to enable accurate evaluation of the S.I.R. requirements by an independent laboratory. For internal laboratory testing for S.I.R, supplier shall obtain the written agreement form Jabil purchase site.

6.18. CLEANLINESS REQUIREMENTS

6.18.1 PCBs shall be free of fiberglass dust; process associated residues, or any other foreign materials.

6.18.2 PCBs shall have a maximum ionic contamination of 6.0 micro grams NaCl equivalent per square inch of PCB surface as measured by an Alpha Metals Omega Meter or equivalent unless otherwise stated in other supplied specification. When cleanliness testing is performed on an OSP PCB, it must be performed after solder mask application and prior to the application of the oxidation inhibitor. Ionic contamination testing must be performed prior to shipment or prior to OSP application. **Ionic Cleanliness Testing shall be performed prior to Shipment, Post HASL, before solder mask application, and after Inner Layer processing as a process control indicator.** All test data shall be retained for a period of one year and available to Jabil personnel upon request. The supplier shall furthermore include on the Certificate of Conformance supplied with each shipment certification that the product meets the requirement of this specification.

6.19. TREACEABILILITY

6.19.1 The supplier must provide full traceability of the finished PCBs from Jabil back through the supplier manufacturing processes and to the supplier's raw materials suppliers.

6.19.2 The supplier must have a method of finished PCB identification that may be used by Jabil for the purpose of sufficient identification to enable full traceability, as described in section 6.19.1.

6.19.3 The date code, vendor code and UL and/or 94V-0 rating shall be marked on the bottom side of each PCB.

6.20. UL RATING

6.20.1 The supplier's UL rating must conform to 94V-0 requirements unless otherwise specified on the applicable master drawing. Appropriate UL marking must be symbolized on each printed circuit board

6.20.2 A copy of the supplier's UL card must be on file with the SQE assigned to PCBs at the Jabil Supply Chain Management Group. It is the supplier's responsibility to ensure that the current card is the most up to date listing.

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6.21. X'D OUT PCBs WITHIN AN ARRAY

6.21.1 X'd out boards within an array are not permitted unless otherwise stated on the PCB master (Fab) drawing or a receipt of an approved deviation from the appropriate Jabil buyer placing the purchase order prior to shipment.

6.22. PATTERN AND BOARD REPAIR

6.22.1 Unless otherwise specified on the master (Fab) drawing or other supplied specification, all repairs shall be performed in accordance with IPC-7711/7721 and shall meet the requirements therein.

6.22.2 Internal layers 'open' shall not be repaired in any form unless otherwise stated in supplied specification and approval from the Jabil buyer placing the purchase order.

6.22.3 Repair in any form of plated through holes in PCBs shall not be permitted.

6.22.4 Machining errors and extraneous non-plated through holes may be repaired provided the repairs are at least one inch apart, do not penetrate any internal feature, and the repairs do not alter the exterior dimensional features, etc.

6.22.5 A maximum of one open external (outer layer) conductor per side may be repaired. This must not conflict with other supplied requirements. The repair shall be encapsulated with epoxy glue and covered with appropriate solder mask.

6.23. LOT CERTIFICATION/FIRST ARTICLE

6.23.1 If requested by the Jabil buyer or other supplied specifications, the supplier shall provide, with each initial shipment, a first article dimension and visual report including the PCBs used to obtain the data. These shall be clearly segregated and marked as such. Supplier shall provide new part APQP if required in the Purchase Order and or request by site SQE.

6.23.2 The supplier shall provide with each subsequent shipment by date code a dimensional and visual final inspection report from a lot sample representative of the lot, (sample size per purchase order or end customer requirements). The box containing the report shall be clearly marked for identification at receiving inspection.

6.23.3 Both the first article report and the final inspection report shall include all outer PCB dimensions, and a representative sample of all finished holes dimensions – plated and non-plated, including via and tooling holes. In addition, a sample reading of "x" and "y" coordinate dimensions of representative features (various pad centers, tooling holes, component and via holes) shall be included to verify artwork and drilling registration. A Cpk analysis shall be conducted to prove Cpk >= 1.33 and shall be included in the report. The format of the report is left to the discretion of the supplier but must include all dimensional, visual, and lab testing performed. The form must also include management acceptance of the final report.

6.23.4 Upon request, supplier shall supply with each shipment by date code a of representative holes micro-sections of finished PCBs showing drilled hole integrity, plating of hole walls, registration of internal layers, layer stack-up, dielectric thickness, plating thickness, de-smear, and other pertinent features. The supplier should prepare a formal metallurgical report based upon the representative micro-sections and attach the copy to the first article report and/or the final inspection report. The micro-sections shall be prepared from both unsoldered and soldered

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PCBs. In addition, the micro-sections must represent high aspect ratio and other plated through holes.

6.23.5 The supplier shall provide a "Certificate of Compliance" outlining the pre-ship audit results. These shall be provided with each lot shipment and shall be clearly identified with other documents within the shipment.

6.23.6 The supplier shall provide with each shipment/lot a reject (E/T test reject is acceptable) finished PCB for the purpose of use as a solderability sample by Jabil. It is the responsibility of the supplier to clearly identify the sample and package with the reports as indicated above. The samples are not to be counted as shipped product and shall be furnished at the supplier's expense for testing.

6.24. PREPARATION FOR DELIVERY

6.24.1 PCBs shall be packaged flat and in a manner that prevents abrasion, contamination, corrosion, deterioration, moisture absorption, and physical damage. Packaging should also afford the shipment and storage protection necessary to ensure that the PCBs maintain solderability as per shelf-life warranty to PCB surface finishing shall according to Purchase Request and or Purchase Order.

6.24.2 PCB packaging materials shall be free of silicone and sulfur.

6.24.3 A maximum of 25 PCBs may be packaged as a unit wrapped in a moisture proof, vacuum sealed material if the area of the PWB is less than or equal to 25 square inches, or a quantity of 10 PCBs if the area per PCB is greater than 25 square inches. Each package of PCBs shall not exceed 10 pounds in weight. Each package shall contain a R/H indicator (6 spot, 10% - 60% HIC complies with EIA 581) with a minimum of one (1) packet of dry agent/silica gel as a desiccant. The acceptance of the humidity level shall follow the purchase order or requirement for moisture vacuum sealed board.
6.24.3.1 For Immersion Silver board packaging, boards should avoid pack with desiccant, refer to IPC-4553. Unless otherwise specified by customer specification/master drawing and or PO.

6.24.4 Shipping containers shall not exceed 40 pounds and shall conform to the requirements of the National Safe Transit Association (NSTA) Project 3 Test Procedures.

6.24.5 All products whether it be Immersion Gold, OSP, or HASL shall be handled at the suppliers shipping department with gloves. Fingerprints found on final finishes shall be cause for rejection. The immersion silver finishing boards must be pack use sulfur-free paper as separator and also to top and bottom side. Adhesive tape, label, stamp markers and rubber bands are a source of sulfur-bearing compounds and therefore forbidden for use on immersion silver boards. (Unless specified in purchase order or other supplied specifications).

6.24.6 Shipping containers shall identify their contents well enough that they do not have to be opened. The identification markings shall follow the supplier site label requirement.

6.24.7 The PCB packaging and handling requirements shall follow Jabil end-customer specification/requirements or requirements stated in Purchase Request- PR/Purchase Order- PO. If request by Jabil end-customer or stated in Jabil PR/PO, the IPC1601– Printed Board Handling and Storage Guidelines shall be followed as agreed between user and supplier (AABUS). Any deviation/waiver, supplier shall obtain approval from Jabil site that issued the PR/PO.

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6.25. Panel and Fab. Drawing.

6.25.1. When panel and or fab. drawing requested by Jabil, the panel and or fab. drawing provided by suppliers shall contain the information below for proper documentation control and traceability.

6.25.1.1. Supplier/Manufacturer
6.25.1.2. Part number
6.25.1.3. Panel/Fab number and revision
6.25.1.4. Document date
6.25.1.5. Prepared by
6.25.1.6. Approved by
6.25.1.7. Any additional information if specified in PO, etc.

6.25.2. The panel and or fab drawing shall be provided during Engineering Queries/DOE/DFM stage and attached to First Article Inspection report/PPAP. Any deviation shall obtain approval from Jabil purchase site.

7. Risk & Controls

7.0 QUALITY ASSURANCE PROVISIONS

7.1 The manufacturer shall retain records for one year from the end of the life of a product/part number which demonstrate that necessary inspections and testing were performed on Jabil product and that in-process repairs and rework were accomplished, re-inspected and evaluated to be free from impacts to 3F (Fit, Form and Function). These records shall be made available to Jabil upon request.

7.2 The manufacturer shall retain on file for one year from the end of the life of a product/part number micro-sections which are representative of the processes used to manufacture Jabil product. These micro-sections and relevant records shall be traceable to Jabil part numbers and date codes and shall be available to Jabil upon request.

7.3 The manufacturer shall perform reliability testing at a minimum of once per quarter on a product representative of Jabil materials and construction. These tests shall include, but are not limited to:

7.3.1 Moisture Resistance testing in accordance with MIL-STD-202, Method 103B, and or IPC-TM-650 for non MIL product.

7.3.2 Thermal Cycling in accordance with MIL-PRF-55110 and or IPC-TM-650 for non MIL product. The manufacturer shall retain records of test results for a period not less than one year from the end of the life of a product/part number, and shall be made available to Jabil upon request.

7.4 Manufacturing processes used to produce Qualification Samples shall be used to produce Production Lots. Process deviations, which have a material effect on the construction, performance, or reliability of the PCBs, shall have the prior written approval of Jabil.

7.5 Following Supplier Qualification, the supplier shall submit to the Jabil SQE in Supply Chain Management Group a process flow plan which includes major process steps and control and validation points. Jabil reserves the right of periodic audit of this plan.

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7.6 Rejected PCBs may, at Jabil's option, be evaluated by a Material Review Board. An acceptance decision by this board is for one lot only; it does not provide revised acceptance criteria for future shipments.

7.7 Jabil reserves the rights with appropriate notice to source inspect for Jabil product and may, at Jabil's option, repeat any of the inspection or tests contained in this specification.

7.8 The supplier will be responsible to maintain on a monthly basis manufacturing data to support the control of the manufacturing process. Shall provide to Jabil SQE if request for review and audit.

7.9 As it is not required per this specification, it is highly recommended that the supplier implement the use of conformance coupons on all production panels. It is not the intent of Jabil to demand this requirement but to suggest an alternative to reduce cost by not using acceptable product for conformance destructive testing. The format of the conformance coupons is left to the discretion of the supplier but must be representative of the product and technology being manufactured in the lot.

7.10 The potential risk of not implementing the documented process which may lead to PCB fabrication specifications/requirements were not communicated and executed by Jabil division/site and supplier.

8. Revisions History & Change Details: *Go back to cover page – click **HERE***

Rev	Release Date	Author (s)	Change Details
A	05/20/97	Unknown	Update and changed from 4-ME10-1000-014-G
B	12/21/99	Bob Davison	Rewrite for extended quality and current demand
C	10/22/09	HS Tiu	Rewrite for extended quality to match current need Change of site coding from 04 to 00 and rename
D	04/23/10	HS Tiu	Update for to section 5.1, 5.2, 5.3 & 6.2 for obsolete reference standard.
E	9/29/10	HS Tiu	Update for 5. 1 5.3, 6.3, 6.4, 6.5, 6.8, 6.10 & 6.15 to align and reference to IPC standard.
F	JAN/30/13	HS Tiu	Update 5.2 to include IPC standardIPC1601, IPC9151C, IPC1710A, Add 6.3.9, revise 6.23.1, 6.23.2, 6.23,4 & 7.1
G	14 Dec 2015	HS Tiu	Updated 6.1.3, 6.6.1
H	30 Mar 2018	HS Tiu	Update 5.2.1, 6.24.7 & 7.10 with new document format. Update 6.8.6.3 – nickel minimum thickness 118 micro-inches.
I	25 May 2018	HS Tiu	Update 6.8.6.3 – nickel plating thickness shall be minimum of 118 micro-inches and maximum of 236 micro-inches per IPC4552.

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